الفرقة الثانية

Tanta University
Faculty of Engineering
Dept. of Computer & Control Eng.
Subject: Computer Architecture

Date: 26/6/2014
Time allowed: 180 Min.
Full Mark: 100 Mark
Final Term Exam (2nd Semester)

Answer The Following Questions (ملحوظة هامة: الأسئلة في ورقتين)

The First Question

(a) What is wrong with the following register transfer statements:

1. xT: AR ← AR', AR ← 0
2. yT: $R_1 \leftarrow R_2$, $R_1 \leftarrow R_3$
3. zT: PC ← AR, PC ← PC + 1

(b) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages.

S	$C_{in} = 0$	$C_{in} = 1$
0	$D = A + B$ (add)	$D = A + 1$ (increment)
1	$D = A - 1$ (decrement)	$D = A + \overline{B} + 1$ (subtract)

(c) The 8-bit registers AR, BR, CR, and DR initially have the following values:
AR = 11110010, BR = 111111, CR = 10111001 , DR = 11101010.
Determine the 8-bit values in each register after the execution of the following sequence of microoperations.

AR ← AR + BR	Add BR to AR
CR←CR ∧ DR, BR←BR+1	AND DR to CR, increment BR
AR ← AR - CR	Subtract CR from AR

The Second Question

(a) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?

(b) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

1. How many bits are there in the operation code, the register code part, and the address part?
2. Draw the instruction word format and indicate the number of bits in each part.
3. How many bits are there in the data and address inputs of the memory?

(c) A computer uses a memory of 65,536 words with eight bits in each word. It has the following registers: PC, AR, TR (16 bits each), and AC, DR, IR (eight bits each). A memory-reference instruction consists of three words: an 8-bit operation-code (one

word) and a 16-bit address (in the next two words). All operands are eight bits. There is no indirect bit.

1. Draw a block diagram of the computer showing the memory and registers.
2. Draw a diagram showing the placement in memory of a typical three-word instruction and the corresponding 8-bit operand.
3. List the sequence of microoperations for fetching a memory reference instruction and then placing the operand in DR. Start from timing signal T_0.

The Third Question

(a) How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is

1. A computational type requiring an operand from memory;
2. A branch type

(b) Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical results.

(3 + 4)[10 (2 + 6) + 8]

(c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect (e) index with R1 as the index register.

The Fourth Question

(a) What is the purpose of the IP/EIP register?

(b) Find the memory address of the next instruction executed by the microprocessor, when operated in the real mode, for the following CS:IP combinations:

1. CS = 1000H and IP = 2000H
2. CS = 2000H and IP = 1000H

(c) Protected mode memory addressing allows access to which area of the memory in:

1- The **80286** microprocessor

2- The Pentium II microprocessor.

With my best wishes